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20.USB WIFI-(option)

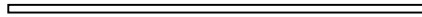
21.MIPI Interface

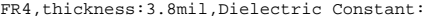
22.DTV-(Reserve)

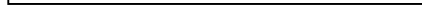
23.HDMI IN

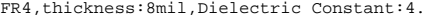
24.VGA OUT

6 LAYERS PCB STACK


TOP(Signal1)  Cu,thickness:0.7mil,Plating to 1oz


GND1  FR4,thickness:3.8mil,Dielectric Constant:4.3

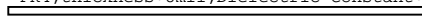
POWER  Cu,thickness:1.5mil, 1oz

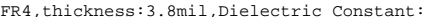
 FR4,thickness:8mil,Dielectric Constant:4.3

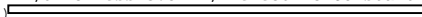
FR4,thickness:adjust thickness according to the thickness of board ,Dielectric Constant:4.3

Signal2  Cu,thickness:1.5mil, 1oz

GND2  FR4,thickness:8mil,Dielectric Constant:4.3

 Cu,thickness:1.5mil, 1oz

BOTTOM(Signal3)  FR4,thickness:3.8mil,Dielectric Constant:4.3

 Cu,thickness:0.7mil,Plating to 1oz



福州瑞芯微电子有限公司

Title: Index

File: RK3288_BOX_Ref

REV:3.0

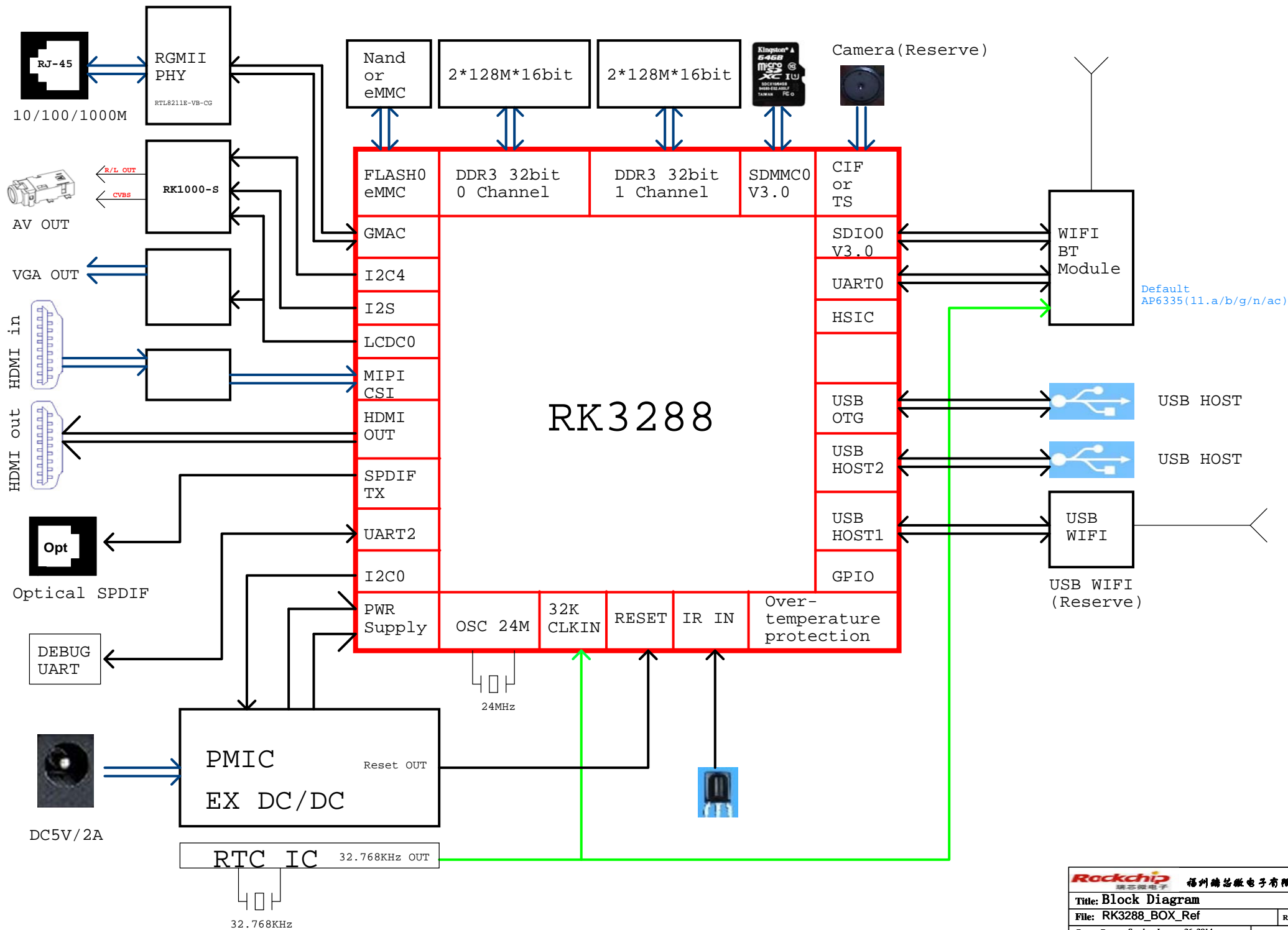
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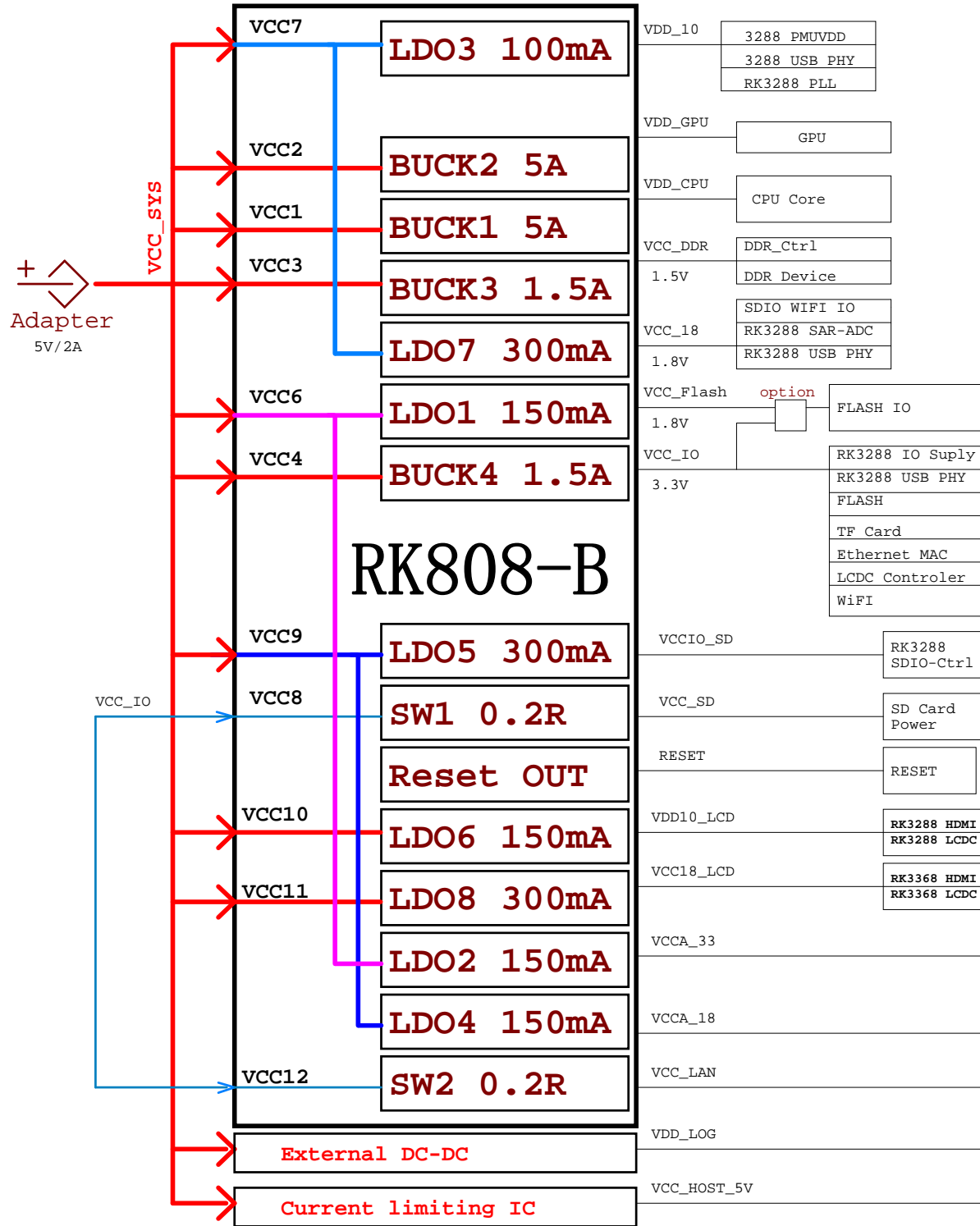
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Modify Date: Tuesday, March 21, 2017

Page Total: 24

Version	Date	Author	Change Note	Approved
V2.0	20170207	LCH	Update	

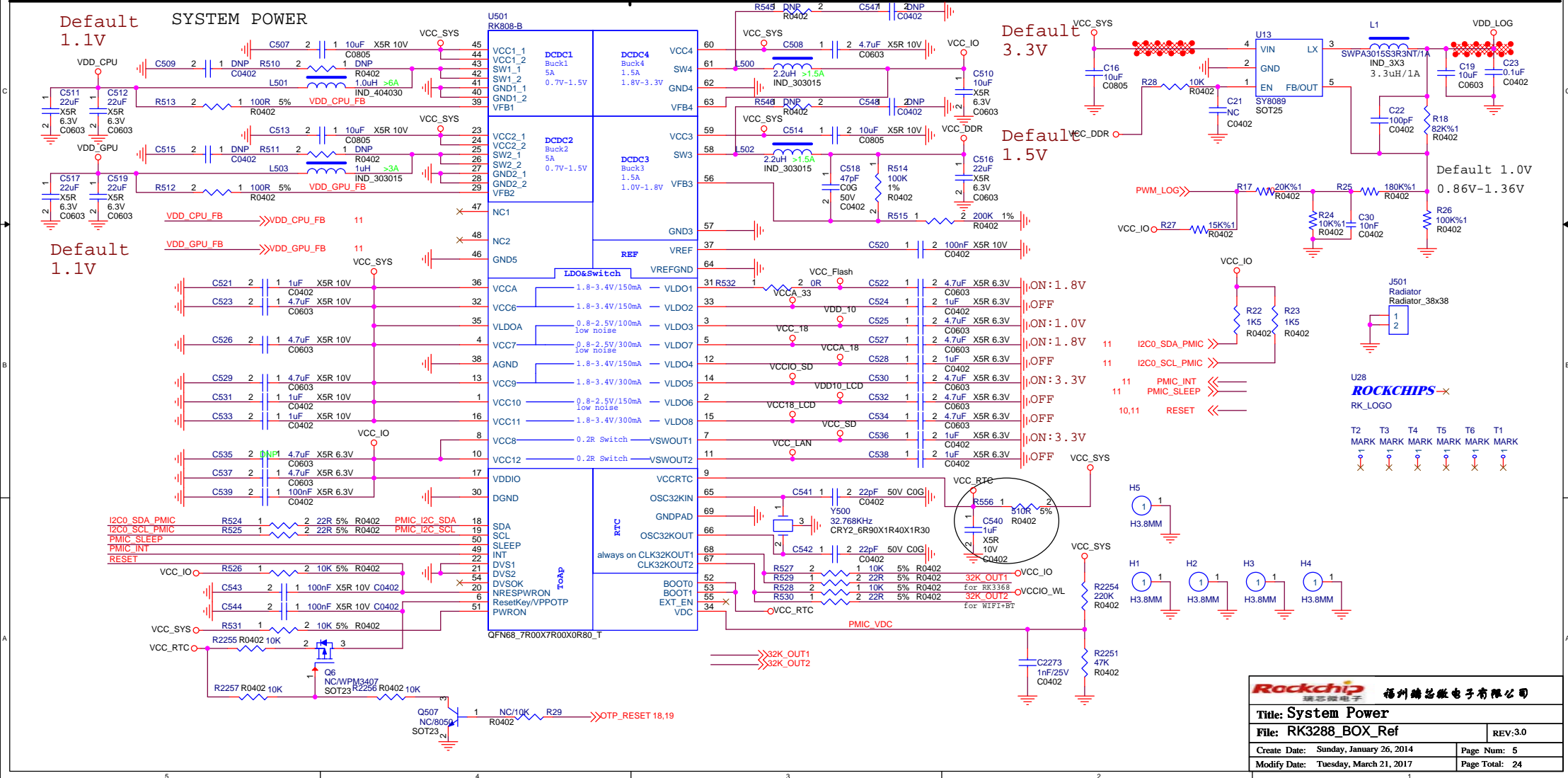
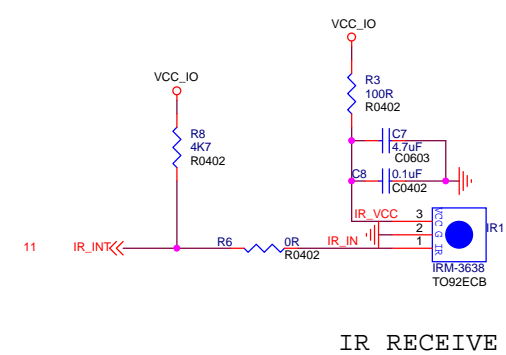
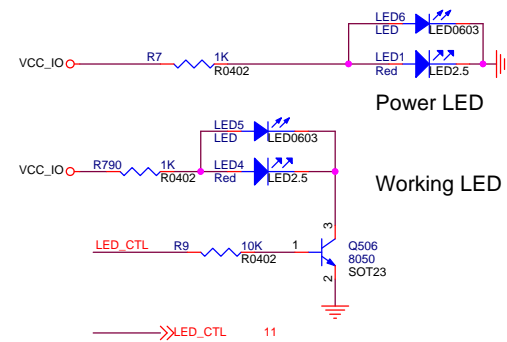
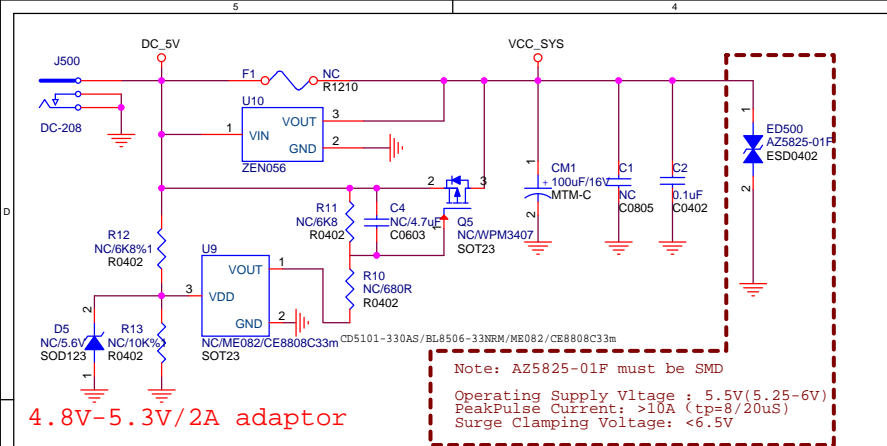


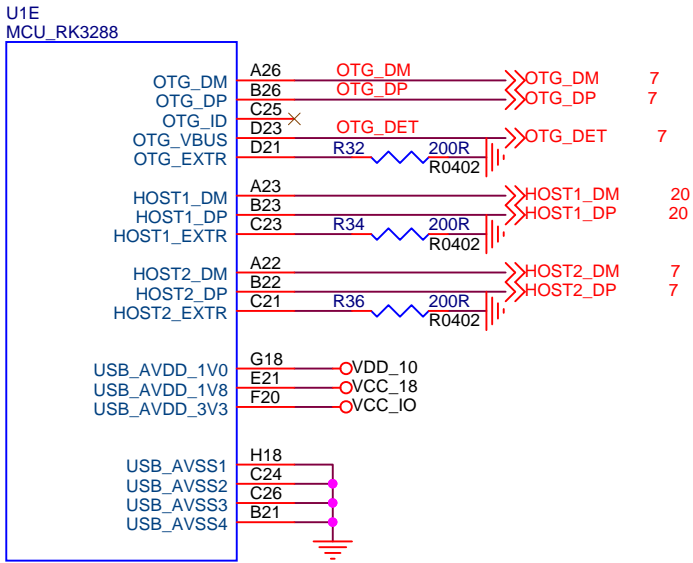


Power up Timing

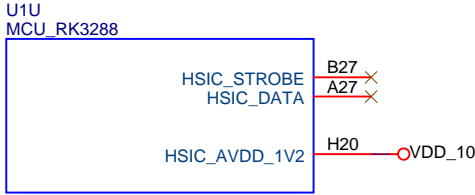
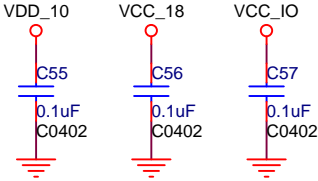
PowerName	RK808-B Channel	timer 2mS	Default voltage	Normal voltage
VDD_10	LDO3	Slot:1	1.0V	1.0V
VDD_CPU	BUCK1	Slot:2	1.1V	DVFS
VDD_GPU	BUCK2	Slot:3	1.1V	DVFS
VDD_LOG	External DC-DC	Slot:4A	1.0V	DVFS
VCC_DDR	BUCK3	Slot:3	1.5V	1.5V
VCC_18	LDO7	Slot:3	1.8V	1.8V
VCC18_FLASH	LDO1	Slot:4	1.8V	1.8V
VCC_IO	BUCK4	Slot:4	3.3V	3.3V
VCCIO_SD	LDO5	Slot:5	3.3V	1.8V or 3.3V
VCC_SD	SW1	Slot:5	3.3V	3.3V
Reset		16*2mS+50mS		
VDD10_LCD	LDO6	OFF	0V	1.0V
VCC18_LCD	LDO8	OFF	0V	1.8V
VCCA_33	LDO2	OFF	0V	3.3V
VCCA_18	LDO4	OFF	0V	1.8V
VCC_LAN	SW2	OFF	0V	3.3V

SPDIF
RK3288 I2S
RK1000-S
Audio Line Driver IC
RK3288 LCDC
RK1000-S
Ethernet PHY
Logic
USB HOST
USB HOST



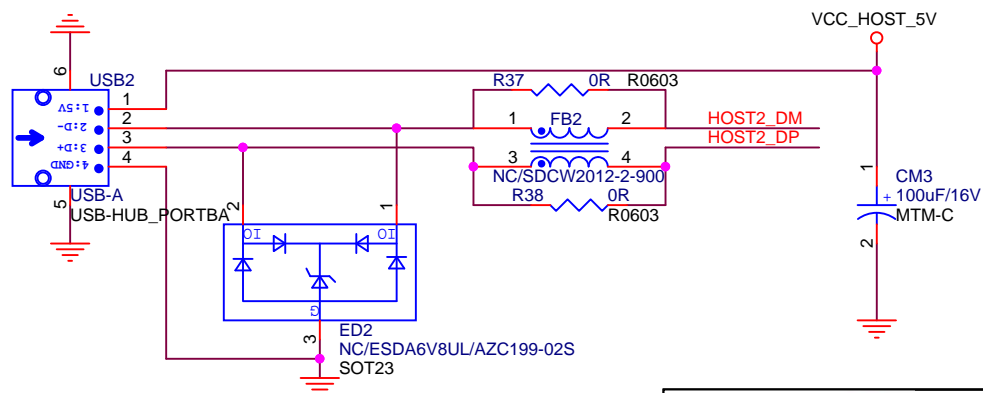
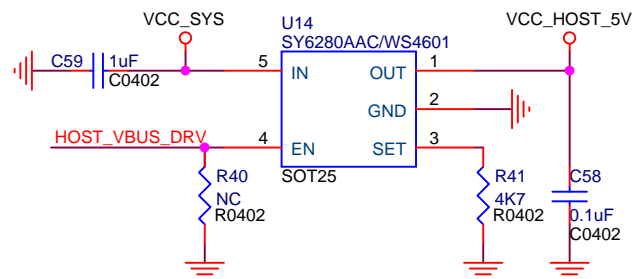
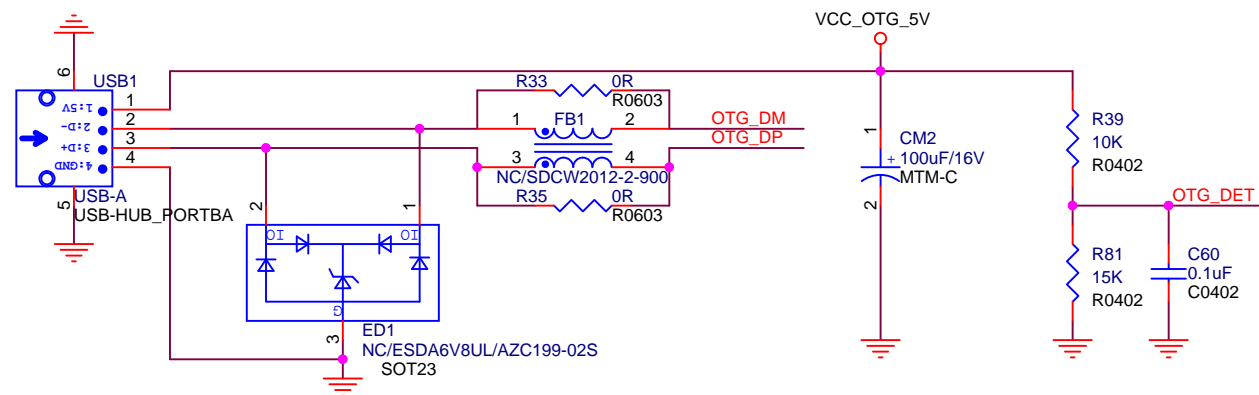
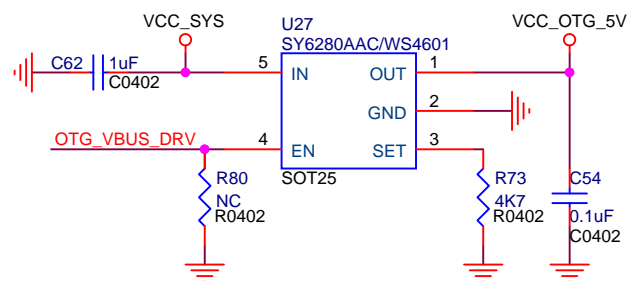


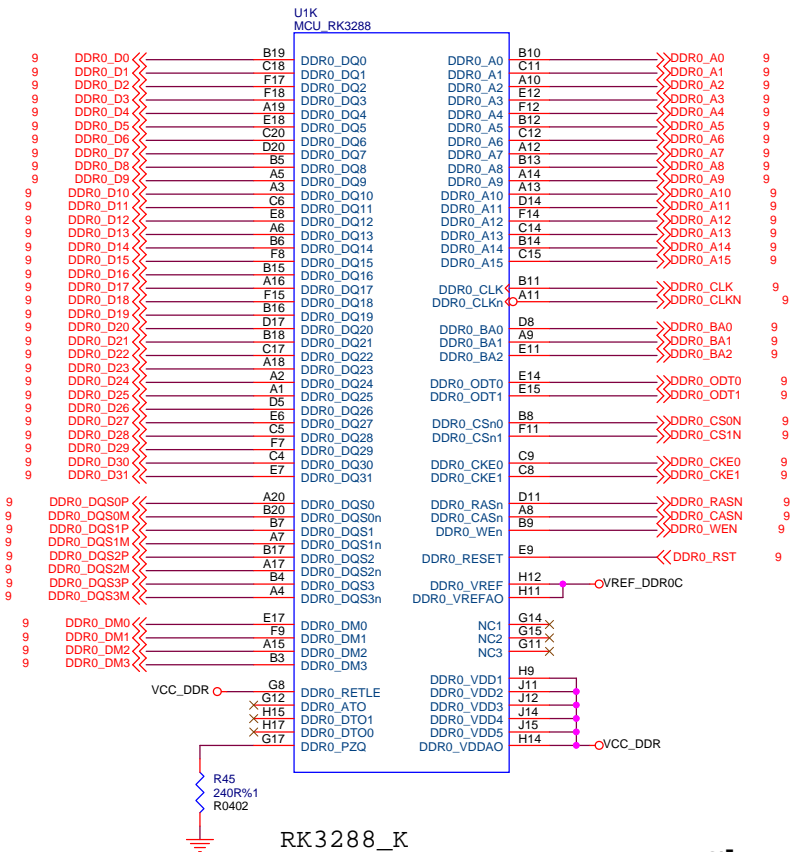
RK3288_E



RK3288_U

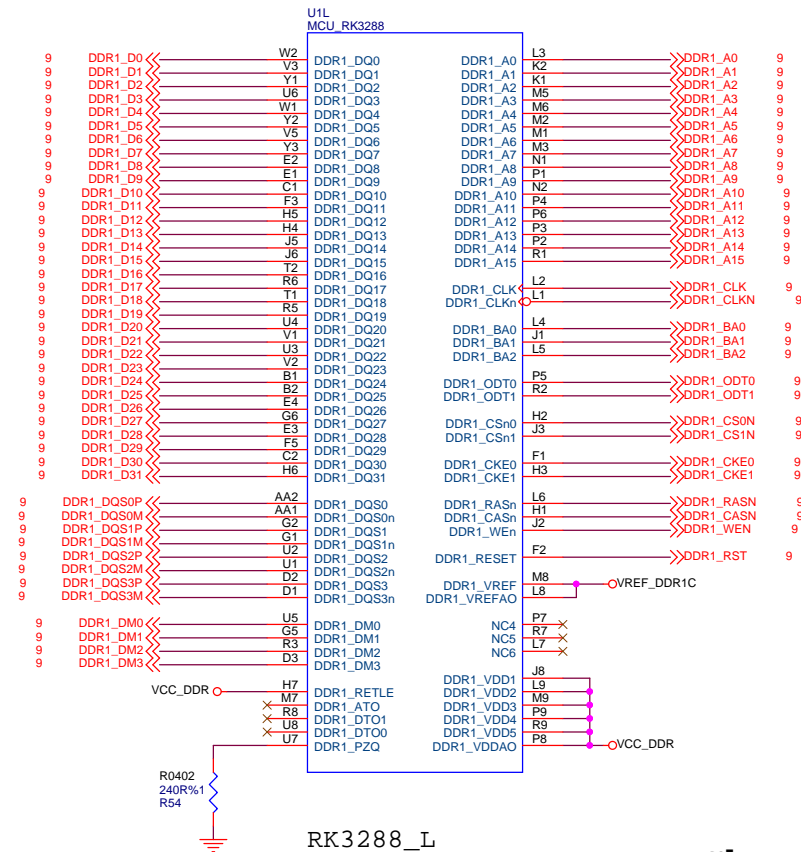
OTG_DM >> OTG_DM 6
 OTG_DP >> OTG_DP 6
 OTG_DET >> OTG_DET 6
 HOST2_DM >> HOST2_DM 6
 HOST2_DP >> HOST2_DP 6
 HOST_VBUS_DRV >> HOST_VBUS_DRV 11
 OTG_VBUS_DRV >> OTG_VBUS_DRV 11





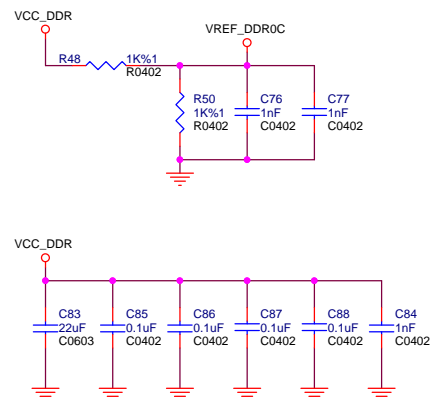
RK3288_K

Channel 0



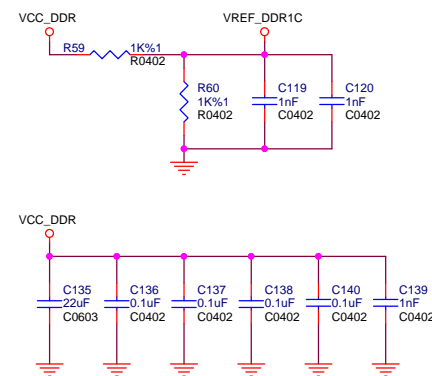
RK3288_L

Channel 1



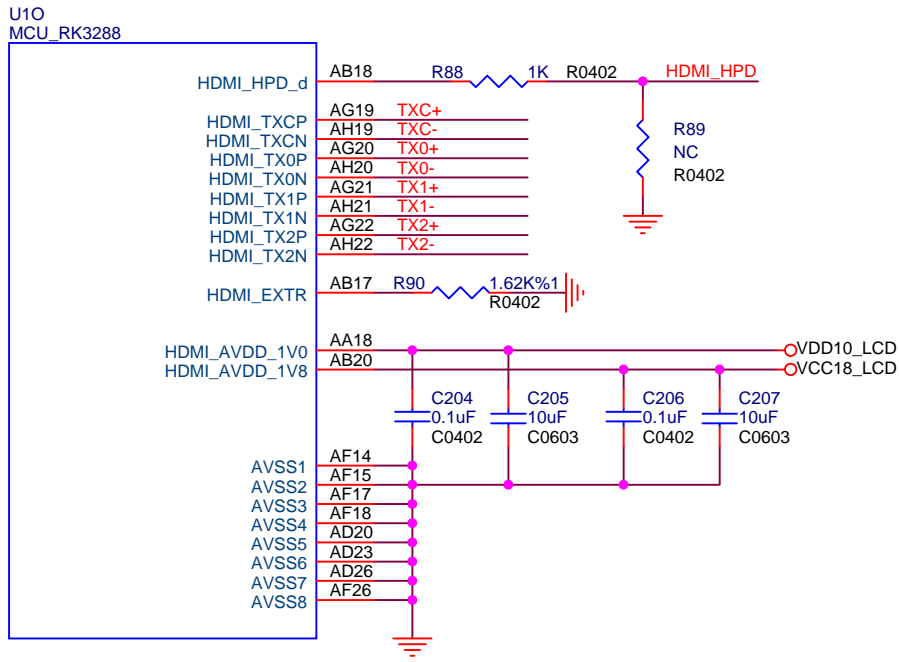
DDR0 FILTER

Note:
These termination resistors must be placed in the middle of trace, and the termination resistor of CLK must be placed in the bifurcation point.

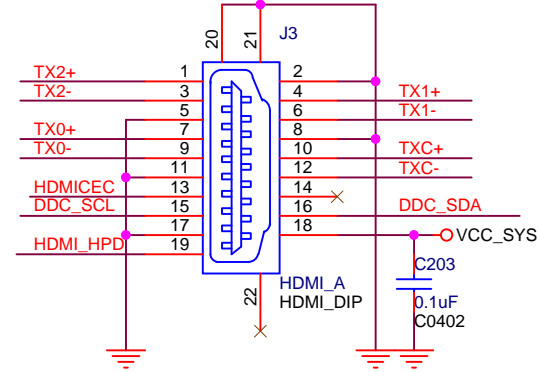
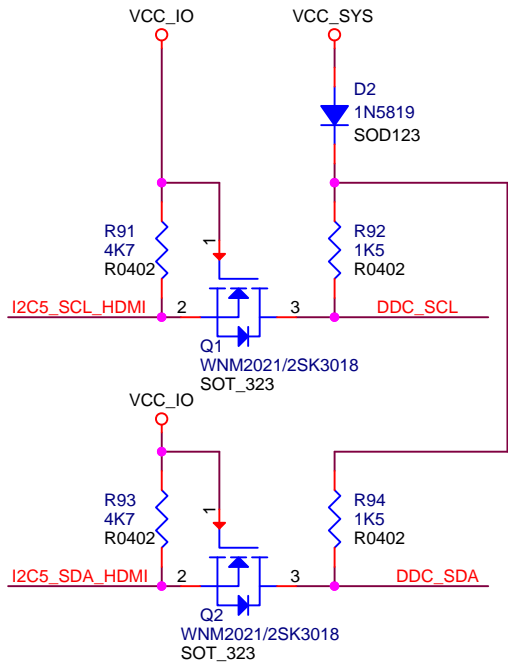
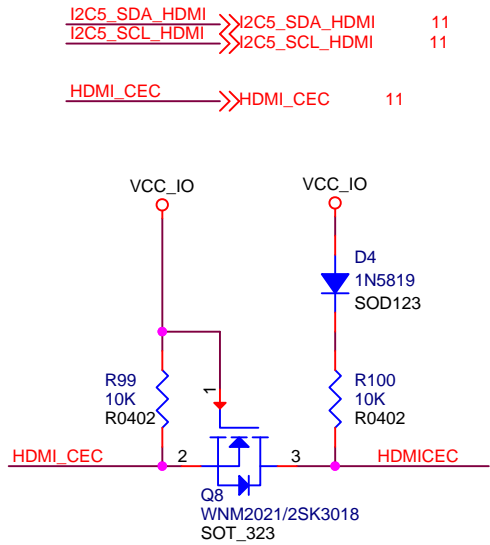


DDR1 FILTER

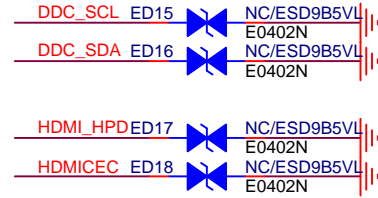
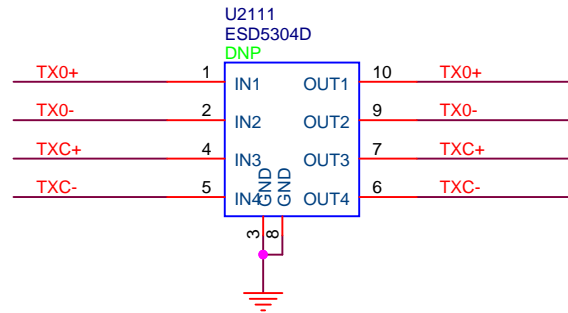
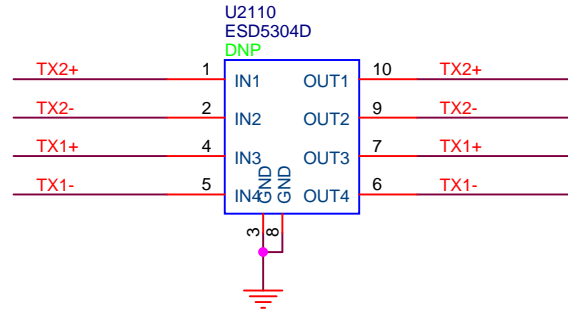
Note:
These termination resistors must be placed in the middle of trace, and the termination resistor of CLK must be placed in the bifurcation point.



RK3288_O

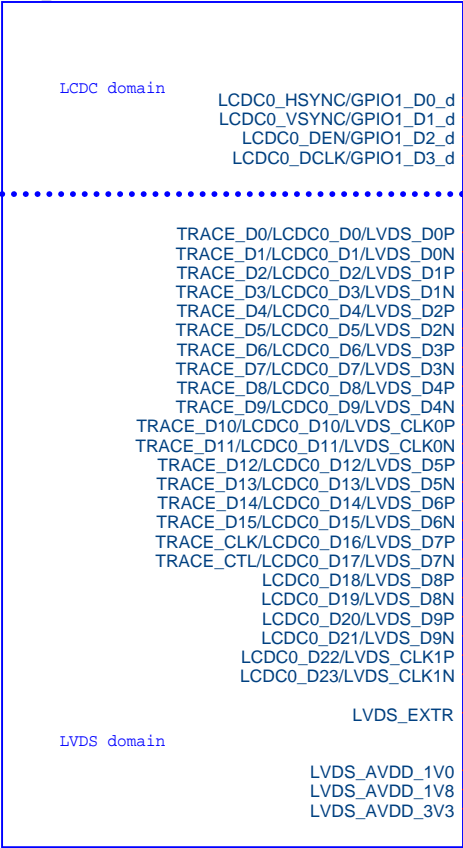


HDMI OUT



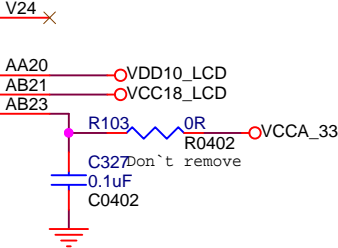
 瑞芯微电子		福州瑞芯微电子有限公司	
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U1A
MCU_RK3288



RK3288_A

AA23	LCD_HSYNC
AB24	LCD_VSYNC
AA22	LCD_DEN
AA24	LCD_CLK
T27	LCD_D0
T28	LCD_D1
U27	LCD_D2
U28	LCD_D3
W27	LCD_D4
W28	LCD_D5
Y27	LCD_D6
Y28	LCD_D7
AA27	LCD_D8
AA28	LCD_D9
V27	LCD_D10
V28	LCD_D11
U25	LCD_D12
U26	LCD_D13
V25	LCD_D14
V26	LCD_D15
AA25	LCD_D16
AA26	LCD_D17
AB27	LCD_D18
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AC25	LCD_D20
AC26	LCD_D21
Y25	LCD_D22
Y26	LCD_D23



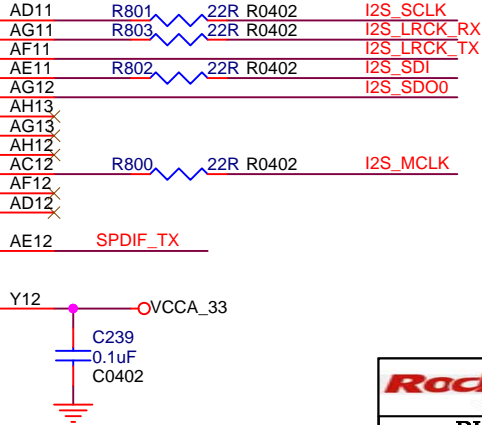
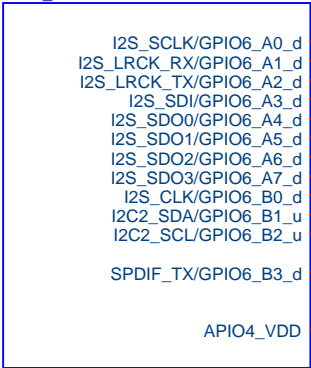
LCD_HSYNC	LCD_HSYNC	14,24
LCD_VSYNC	LCD_VSYNC	14,24
LCD_DEN	LCD_DEN	24
LCD_CLK	LCD_CLK	14,24

LCD_D0	LCD_D0	24
LCD_D1	LCD_D1	14,24
LCD_D2	LCD_D2	14,24
LCD_D3	LCD_D3	14,24
LCD_D4	LCD_D4	14,24
LCD_D5	LCD_D5	14,24
LCD_D6	LCD_D6	14,24
LCD_D7	LCD_D7	14,24
LCD_D8	LCD_D8	24
LCD_D9	LCD_D9	14,24
LCD_D10	LCD_D10	14,24
LCD_D11	LCD_D11	14,24
LCD_D12	LCD_D12	14,24
LCD_D13	LCD_D13	14,24
LCD_D14	LCD_D14	14,24
LCD_D15	LCD_D15	14,24
LCD_D16	LCD_D16	24
LCD_D17	LCD_D17	14,24
LCD_D18	LCD_D18	14,24
LCD_D19	LCD_D19	14,24
LCD_D20	LCD_D20	14,24
LCD_D21	LCD_D21	14,24
LCD_D22	LCD_D22	14,24
LCD_D23	LCD_D23	14,24


I2S_SCLK	I2S_SCLK	14,23
I2S_LRCK_RX	I2S_LRCK_RX	14,23
I2S_LRCK_TX	I2S_LRCK_TX	14
I2S_SDI	I2S_SDI	14,23
I2S_SDO0	I2S_SDO0	14
I2S_MCLK	I2S_MCLK	14,23

SPDIF_TX	SPDIF_TX	15
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U1I
MCU_RK3288



RK3288_I



福州瑞芯微电子有限公司

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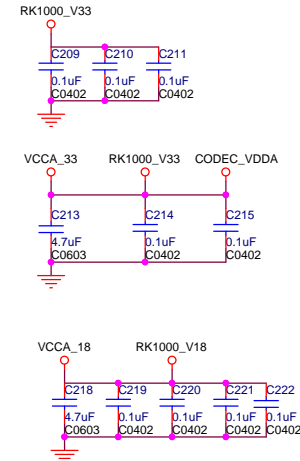
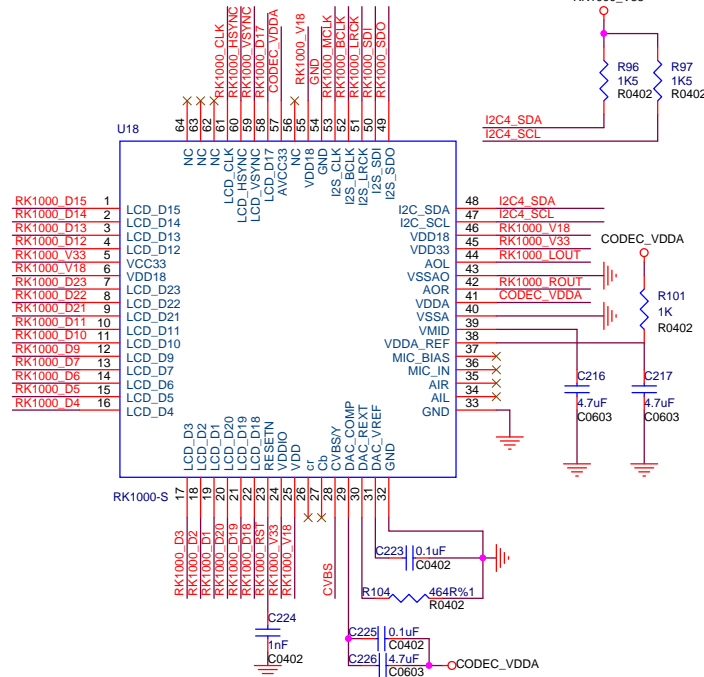
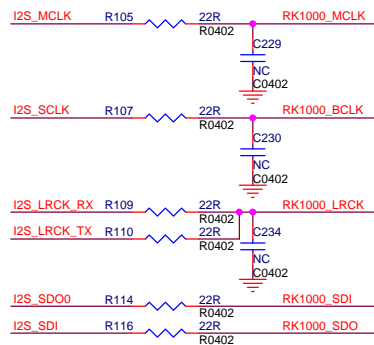
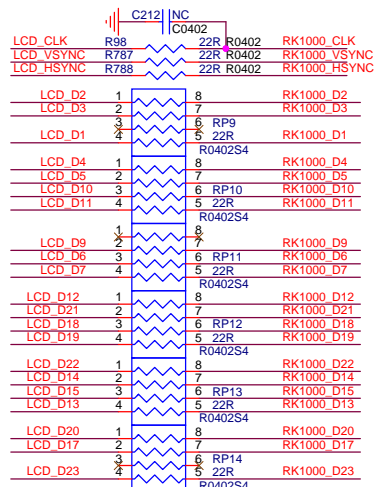
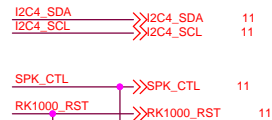
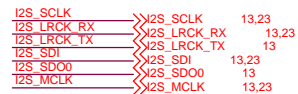
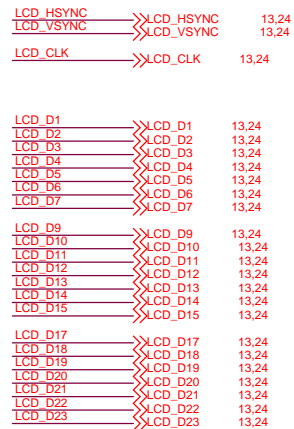
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Modify Date: Tuesday, March 21, 2017

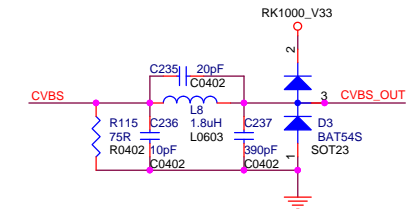
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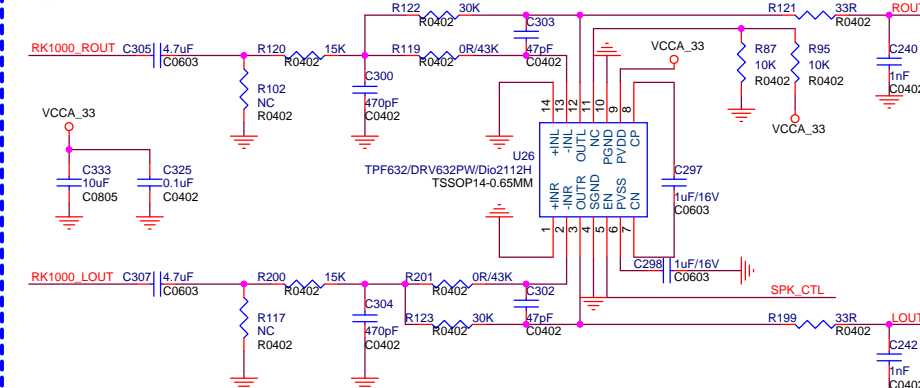
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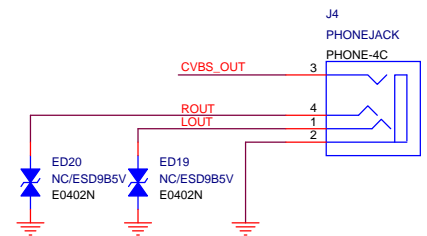
RK1000-S POWER



R/L OUT



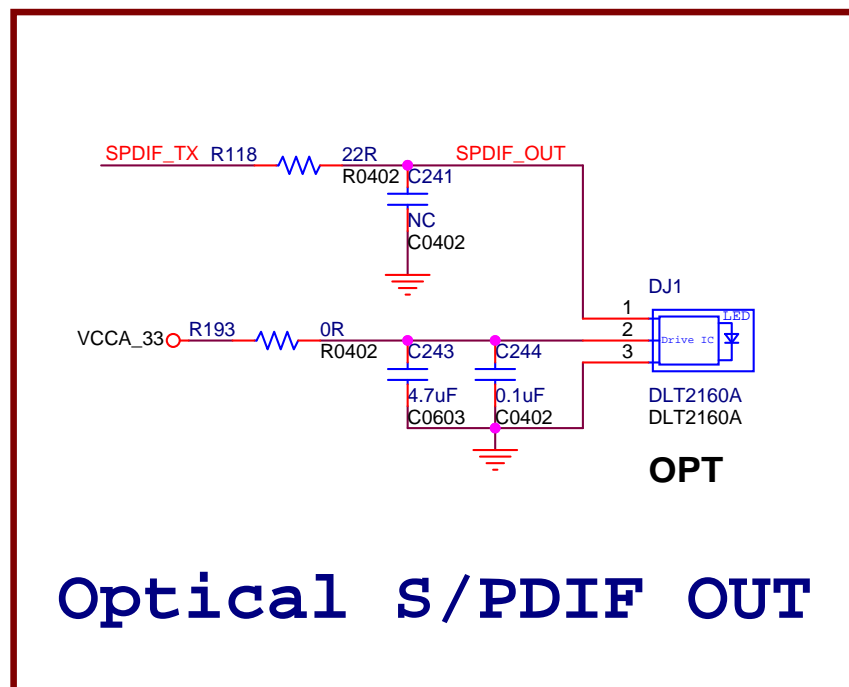
2-Vrms Audio Line Driver




AV OUT

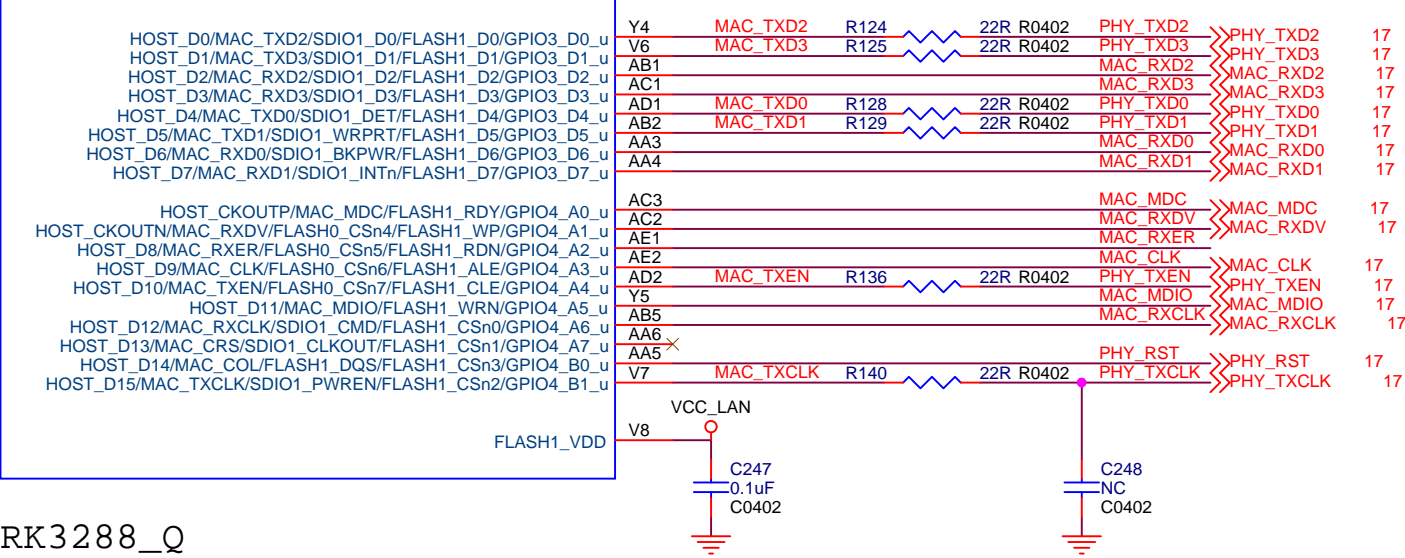
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SPDIF_TX → SPDIF_TX 13

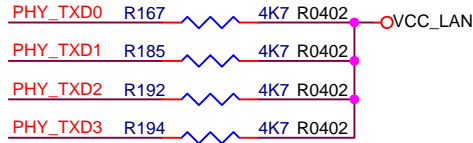
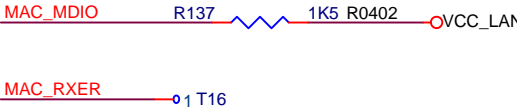


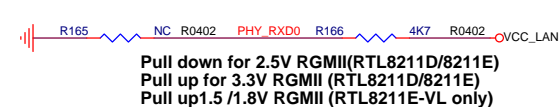
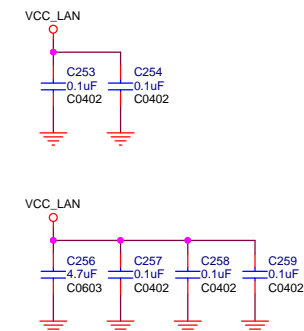
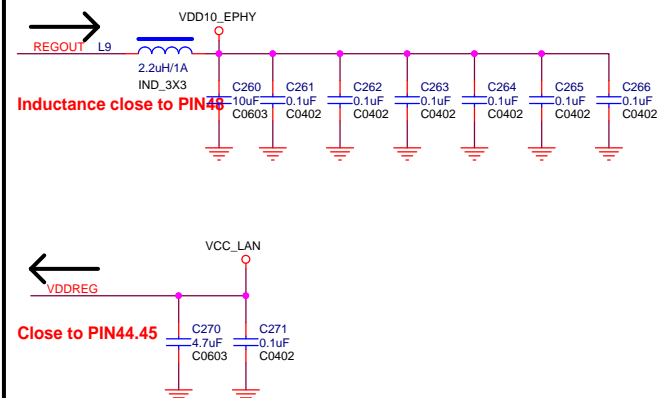
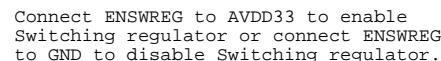
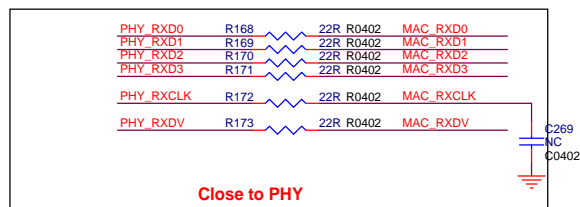
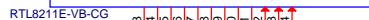
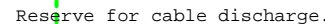
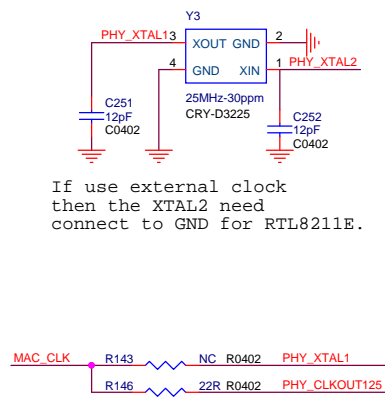
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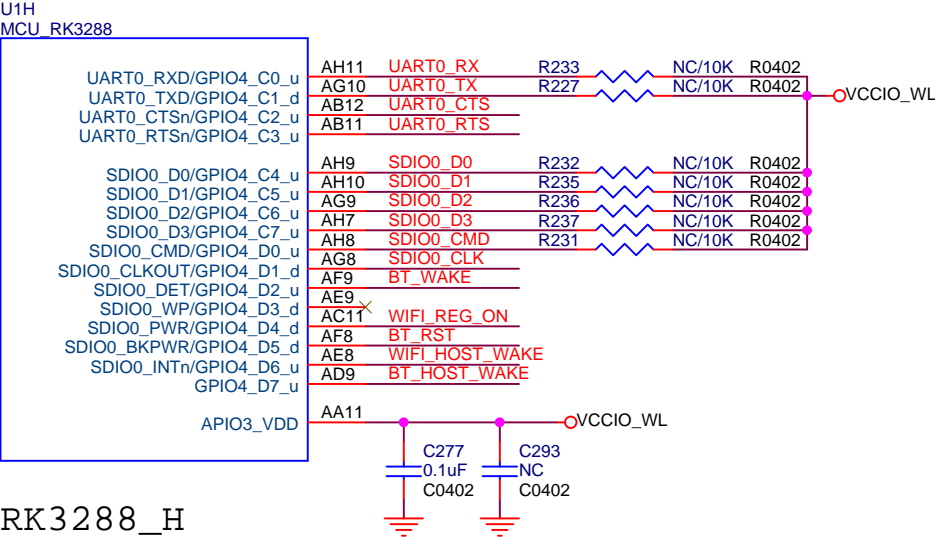
U1Q
MCU_RK3288



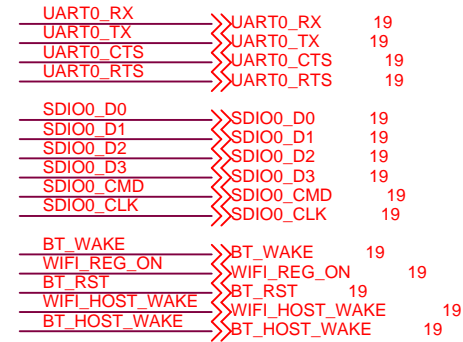
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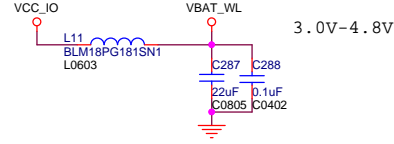
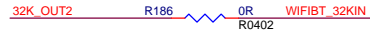
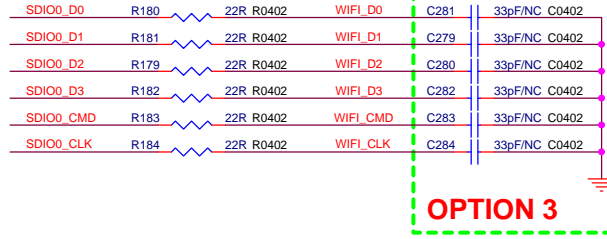
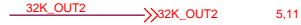
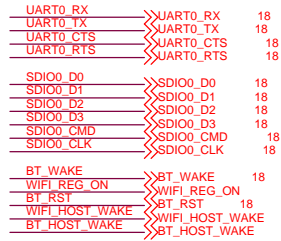




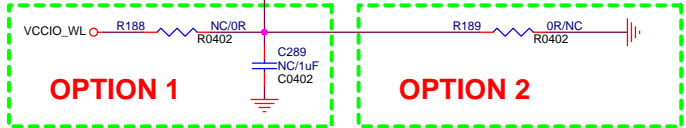
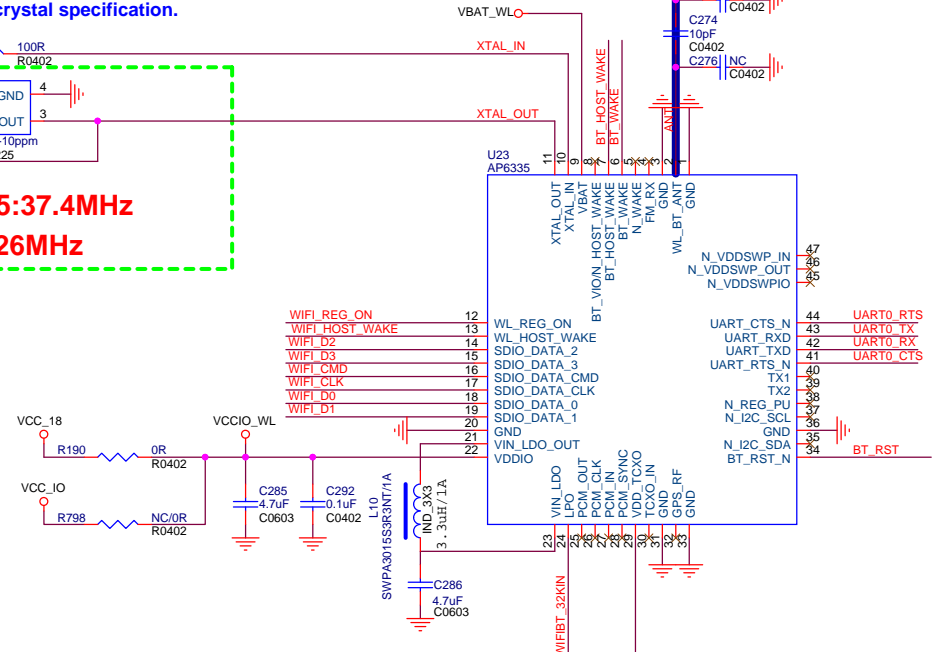
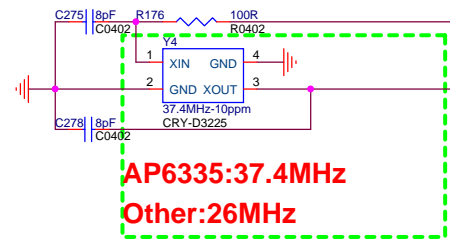


RK3288_H



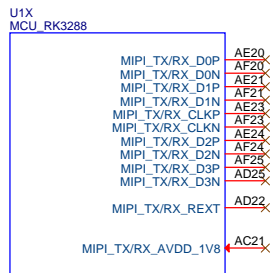
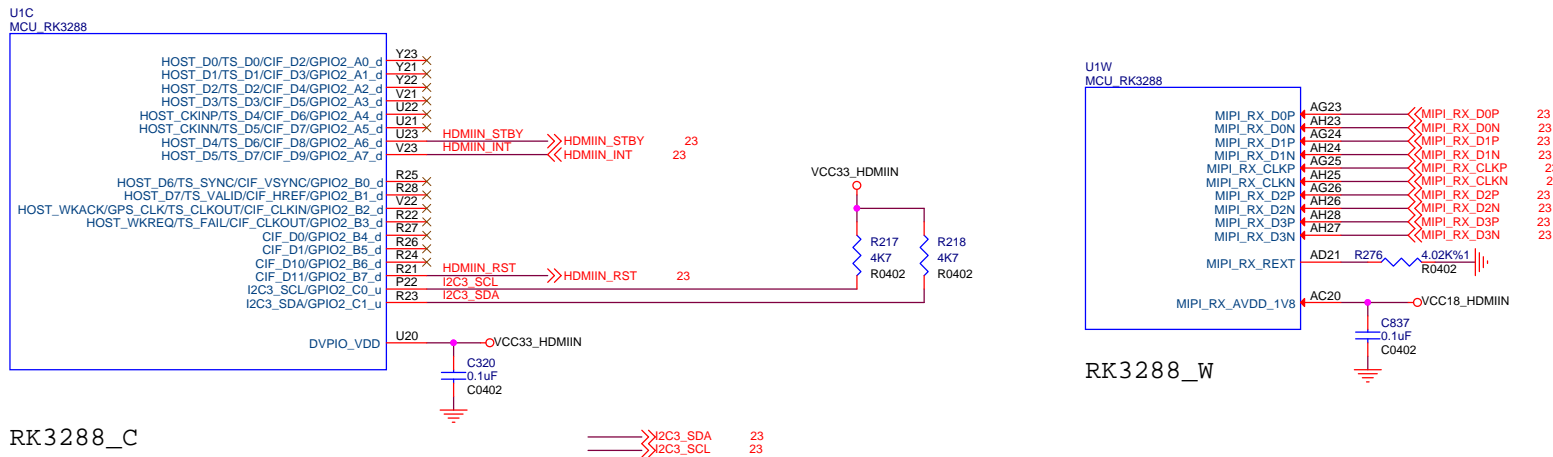


Note:
Adjusted the load capacitance
according to the crystal specification.

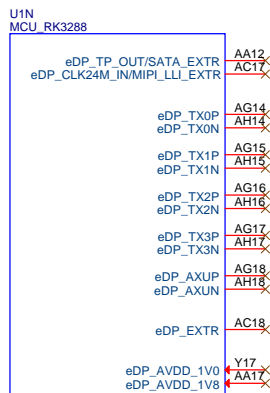


OPTION	WIFI				BT4.0	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181		Yes				26MHz	1.71~3.6V
AP6212		Yes			Yes	26MHz	1.71~3.6V
XZ3538		Yes			Yes	26MHz	1.71~3.6V
XZ3660	Yes	Yes		Yes	Yes	26MHz	1.2~2.9V
AP6330	Yes	Yes		Yes	Yes	26MHz	1.2~2.9V
AP6335 (Default)	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71~3.63V

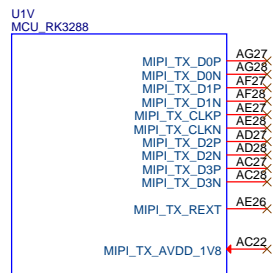
OPTION	1	2	3
AP6181	DNP	DNP	DNP
AP6212	DNP	DNP	DNP
XZ3538	DNP	DNP	DNP
XZ3660	DNP	DNP	DNP
AP6330	DNP	DNP	DNP
AP6335 (Default)	DNP	Paste	Paste



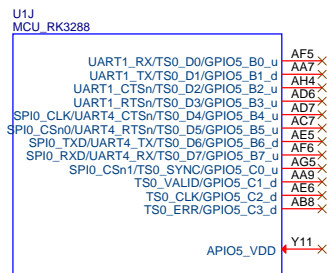
RK3288_X



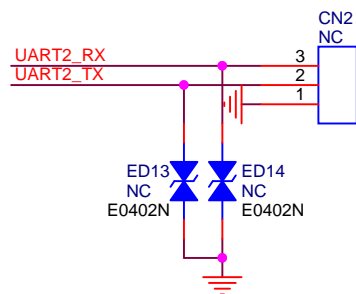
RK3288_N



RK3288_V



RK3288_J





LCD_HSYNC >> LCD_HSINC 13,14
 LCD_VSYNC >> LCD_VSINC 13,14
 LCD_DEN >> LCD_DEN 13
 LCD_CLK >> LCD_CLK 13,14

LCD_D0 >> LCD_D0 13
 LCD_D1 >> LCD_D1 13,14
 LCD_D2 >> LCD_D2 13,14
 LCD_D3 >> LCD_D3 13,14
 LCD_D4 >> LCD_D4 13,14
 LCD_D5 >> LCD_D5 13,14
 LCD_D6 >> LCD_D6 13,14
 LCD_D7 >> LCD_D7 13,14
 LCD_D8 >> LCD_D8 13
 LCD_D9 >> LCD_D9 13,14
 LCD_D10 >> LCD_D10 13,14
 LCD_D11 >> LCD_D11 13,14
 LCD_D12 >> LCD_D12 13,14
 LCD_D13 >> LCD_D13 13,14
 LCD_D14 >> LCD_D14 13,14
 LCD_D15 >> LCD_D15 13,14
 LCD_D16 >> LCD_D16 13
 LCD_D17 >> LCD_D17 13,14
 LCD_D18 >> LCD_D18 13,14
 LCD_D19 >> LCD_D19 13,14
 LCD_D20 >> LCD_D20 13,14
 LCD_D21 >> LCD_D21 13,14
 LCD_D22 >> LCD_D22 13,14
 LCD_D23 >> LCD_D23 13,14

>>VGA_I2C_SDA 11
 >>VGA_I2C_SCL 11
 >>XN223_PWN 11
 >>XN223_PWREN 11

